

ABSTRACT

The invention provides a decoding circuit and a decoding method of a Viterbi decoder. The decoding circuit of the Viterbi decoder includes a branch metric unit, an add-compare-select unit and a path memory unit. The path memory unit
5 includes a data string controller, a trace write-in register array, an idling register array and a decoding register array. In this invention, a run length limited code is used for effectively solving the problem of generating a complicated trellis diagram after the trellis diagram of the Viterbi decoder is subjected to a longitudinal arrangement. In addition, the register array can perform other operations at different time.
10 Accordingly, a high decoding speed of the Viterbi decoder can be achieved without requiring a lot of registers for data processing.

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